Experimental Methodology –

In order to set up for the lab, the team needed a computer running ModelSim in order to simulate VHDL code compiled in Quartus Prime. Once this code was written in QP, it was then converted into a symbol file and entered into a schematic. After the schematic was finished, the team compiled the file and simulated it in ModelSim to get the following results.

Results –

Graphical user interface, treemap chart

Description automatically generated with medium confidence

ModelSim simulation of VHDL coded decoder with inputs 0 and 0.

Graphical user interface

Description automatically generated

ModelSim simulation of VHDL coded decoder with inputs 0 and 1.

Graphical user interface

Description automatically generated

ModelSim simulation of VHDL coded decoder with inputs 1 and 0.

Graphical user interface

Description automatically generated

ModelSim simulation of VHDL coded decoder with inputs 1 and 1.